29. (Added) The device as recited in claim 24, further comprising:

an additional gate conductor interposed between the low-trap-density nitrogen-containing oxide and the semiconductor substrate; and

a gate dielectric arranged interposed between the additional gate conductor and the semiconductor substrate.

REMARKS

Claims 23-29 have been added; therefore, claims 17-29 are pending in the case. Applicants hereby request further examination and reconsideration of the presently claimed application.

Objection to the Drawings:

Receipt of Notice of Draftsperson's Patent Drawing Review, PTO-948, is acknowledged. The objections included in the Notice of Draftsperson's Patent Drawing Review will be addressed in the final, formal drawings to be filed when the application is allowed.

Section 102 Rejections:

Claims 16 and 18 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,596,214 to Endo et al. ("Endo"). These rejections are respectfully traversed, as set forth in more detail below.

The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); MPEP 2131. The cited art does not anticipate the pending claims as will be set forth in more detail below.

The cited art does not describe a semiconductor device having a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor surface. Independent claim 16 recites in part, "a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate." Claim 18, which depends from claim 16, recites all the limitations of claim 16. Endo describes a non-volatile semiconductor memory device (Endo -- Abstract). The memory device described by Endo recites a nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate (Endo -- col. 14, lines 57-60). However, the nitrogen-containing oxide taught by Endo may not be properly construed as the claimed low-trap-density nitrogen-containing oxide for at least the following reasons.

The present Specification recites the desirability of low-trap-densities in the formation of devices having stable operating characteristics (Specification -- pg. 4, lines 8-18). Further, the Specification recites several methods that may lower trap densities. For example: "[t]he N_2O anneal is believed to reduce the trap density of the nitrogen-containing oxide" (Specification -- pg. 6, lines 16-17); "[t]he etch process [may be performed before annealing] . . . in order to reduce the density of any traps which may be introduced . . . during the etch process" (Specification -- pg. 6, line 29 - pg. 7, line 2); and "[t]hermal growth of nitrogen-containing oxide 12 is believed to provide a lower density of interface trap states" (Specification -- pg. 11, lines 27-28). Consequently, the Specification recites the desirability of low trap densities, and discloses several methods that may lower trap densities, and thereby forms the presently claimed product (i.e., the claimed low-trap-density nitrogen-containing oxide).

In contrast, the memory device taught by Endo appears to rely upon trap sites to operate correctly. Endo therefore does not appear to depend on the present use of a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor surface. For example, Endo recites:

> When a voltage is applied between the gate electrode and the semiconductor substrate, electrons exhibit a direct tunneling across the first gate insulating layer for the write-erase operations. The electrons having exhibited the direct tunneling from the channel region are trapped into interfacial States on an interface between the first and second gate insulating layers. (Endo -- col. 7, lines 14-20, emphasis added.)

Endo teaches that a "1" in logic states is created by applying a positive voltage to the gate electrode so electrons will tunnel across the silicon dioxide film. The electrons will remain trapped on the interface of the silicon dioxide and silicon nitride films when zero volts are subsequently applied to the gate electrode (Endo -- col. 2, lines 42-54). Endo repeats numerous times that electrons are trapped into the interface between the silicon dioxide and silicon nitride films. See, for example, Endo col. 6, lines 39-44 and lines 61-64; col. 7, lines 17-20; col. 9, lines 8-12; col. 13, lines 1-4; and col. 13, lines 28-31. Consequently, Endo appears to require trap densities for proper storage function, and thus Endo cannot teach or suggest the claimed low-trap-density films. Endo therefore teaches away from the claimed low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor surface.

Moreover, Endo recites the need to increase the density of trap sites. Within his fifth embodiment, Endo discloses the necessity of increasing trap density, and further recites a method to increase the trap density (Endo -- col. 21, line 44 - col. 22, line 46). For example:

> . . . the increase of the dielectric constant of the second dielectric film 15 requires an increase of the number of the captured electrons at the trap centers . . . The increase in the number of electrons captured or trapped at the trap centers requires an increase of the number of interfacial trap centers . . . In order to achieve the increase of the number of interfacial trap centers for electrons, the silicon particles provide many electron trap centers being available to capture or trap electrons. (Endo -- col. 22, lines 15-28, emphasis added.)

Endo teaches away from methods that may lower trap densities. For example, Endo recites "diffusion regions are formed by . . . annealing . . . [i]t is important that the heat treatment is carried out at a possible low temperature to prevent any deterioration of electrical properties of the second dielectric film." (Endo -- col. 15, lines 13-19.) In contrast, as noted above, the

Specification recites methods to reduce trap-densities. Further, the Specification recites that the methods may require the use of high temperatures. For example, "[the N_20 anneal] involves heating substrate 10 to a temperature greater than about 800 °C in an ambient containing N_20" (Specification -- pg. 13, lines 14-18); and "[t]he etch may be performed . . . at a substrate temperature between about 500 °C and 900 °C" (Specification -- pg. 6, lines 25-28). Therefore, the Specification recites methods to reduce trap-densities that may involve the use of high temperatures. In contrast, Endo teaches use of low temperatures to maintain high trap densities.

Endo neither expressly nor inherently describes the claimed low-trap density nitrogen-containing oxide recited by claim 16; therefore, Endo cannot anticipate claim 16. As such, independent claim 16 is patentably distinct and in condition for allowance. Dependent claims 17-22, including rejected claim 18, are also patentably distinct and in condition for allowance for at least the same reasons as claim 16. Removal of the 35 U.S.C. § 102(b) rejection of claims 16 and 18, and claims dependent therefrom, is respectfully requested.

Section 103 Rejections:

Claims 17, 19, 21, and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo as applied to claim 16 above, and further in view of U.S. Patent 6,015,739 to Gardner et al. (hereinafter "Gardner"). Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo as applied to claim 16 above, and further in view of U.S. Patent 5,994,734 to Chou (hereinafter "Chou"). The rejections of claims 17, 19, 20, 21, and 22 are traversed, as set forth in further detail below.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention, where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine,* 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In *re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992), MPEP § 2143.01. (Emphasis added.) To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka,* 490 F.2d 981, 180 U.S.P.Q.

580 (C.C.P.A. 1974), MPEP § 2143.03. As such, the pending claims are not obvious in view of the cited art for at least the following reasons.

The cited art does not appear to teach or suggest a semiconductor device having a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor surface. As discussed above in reference to the § 102 rejection of claim 16, Endo does not disclose the claimed low-trap-density nitrogen-containing oxide. Claims 17-22, including rejected claims 17, 19, 21, and 22, depend from claim 16 and, therefore, recite all its limitations. The cited art does not remedy the deficiencies of Endo such that all limitations of independent claim 16 are taught or suggested as will be set forth in more detail below.

Gardner teaches a method of making a gate dielectric having a graded gate dielectric. (Gardner -- Abstract). Although Gardner appears to teach a first dielectric film comprising silicon oxide (Gardner -- col. 5, lines 43-45), Gardner does not appear to teach or suggest a semiconductor device having a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor surface as claimed. Further, Gardner provides no motivation to modify Endo such that their combination teaches the claimed low-trap-density nitrogen-containing oxide. Consequently, Gardner cannot remedy the deficiencies of Endo with respect to rejected claim 16 and the claims dependent therefrom.

Chou teaches a modified gate structure for a non-volatile memory device. (Chou -- Abstract). Although Chou appears to teach a first dielectric formed on a substrate (Chou -- col. 2, lines 59-60), Chou does not teach or suggest a semiconductor device having a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor surface as claimed. Furthermore, Chou does not disclose motivation to modify the cited art such that their combination teaches the claimed low-trap-density nitrogen-containing oxide. Therefore, Chou cannot remedy the deficiencies of the cited art with respect to independent claim 16. As a result, Chou cannot remedy the deficiencies of the cited art with respect to rejected claim 20, which depends from claim 16. As such, claim 20 is believed patentably distinct and in condition for allowance.

Further, it is asserted that some of the dependent claims are separately patentable. The cited art teaches away from the proposed combination. It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). It is asserted that dependent claims 21 and 22 are separately patentable. Claim 21 recites in part, "said nitrogen-containing oxide has a thickness of less than about 10 angstroms." Claim 22 recites in part, "said silicon nitride has a thickness of less than or equal to about 10 angstroms." However, Endo teaches away from these limitations.

Endo appears to teach that the thickness of the first and second insulating films must satisfy specific conditions. (Endo -- col. 9, lines 41-49; col. 10, lines 4-10). To satisfy the required conditions "the minimum thickness of the first dielectric film would be 2.5 nanometers" (Endo -- col. 11, lines 2-5) and "50 nanometers in the thickness of the second dielectric film would be the minimum" (Endo -- col. 12, lines 14-16). Therefore, Endo requires minimum thicknesses that are much larger than those claimed. Claim 21 recites the nitrogen-containing oxide is less than about 10 angstroms thick, which is much smaller than the 2.5 nanometers, or 25 angstroms, Endo teaches as a minimum thickness for the first dielectric film. Likewise, claim 22 recites the thickness of the silicon nitride is less than about 10 angstroms, which is much smaller than the 5 nanometers, or 50 angstroms, Endo teaches as a minimum thickness for the first dielectric film. Therefore, Endo teaches away from the limitations presented in claims 21 and 22. Consequently, Endo does not and cannot teach or suggest the limitations recited by dependent claims 21 and 22. As such, claims 21 and 22 are separately patentable.

For at least the reasons cited above, the cited art does not teach or suggest all limitations of any of the pending claims. As such, pending claims 16-22 are patentably distinct from the cited art and thus in condition for allowance. Removal of the §103 rejections of claims 17, 19, 20, 21, and 22 is respectfully requested.

Patentability of Added Claims:

The present amendment adds claims 23-29. The limitations recited by claims 23 and 27 can be found, for example, in the Specification, pg. 12, line 30. Claim 24 recites limitations that can be found, for example, in the Specification, pp. 5-7. Claims 25, 26, 28, and 29 recite limitations that are similar to those in pending claims 17, 18, 19, and 20, respectively. Therefore, claims 23-29 do not present new matter.

Claim 23 depends from claim 16; therefore, it is patentably distinct for at least the same reasons as claim 16 set forth above. Claim 24 is a new independent claim and claims 25-29 depend from claim 24. Claim 24 recites:

> A semiconductor device, comprising: a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate, wherein said low-trap-density nitrogen-containing oxide has a thickness of less than about 10 angstroms; a high-K dielectric having a dielectric constant greater than about 5 arranged upon the nitrogen-containing oxide, wherein said high-K dielectric has a thickness of less than or equal to about 10 angstroms; and a gate conductor arranged above the high K dielectric.

As recited above, the cited art neither teaches nor suggests a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate. As also recited above, the cited art teaches away from the claimed thicknesses. Consequently, added independent claim 24 is patentably distinct and in condition for allowance, as are its dependent claims 25-29.

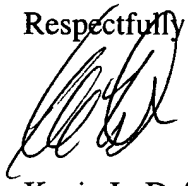
CONCLUSION

In the present response, claims 23-29 have been added. Receipt of Notice of Draftsperson's Patent Drawing Review has been acknowledged. Applicants have also responded to the rejections of claims 16-22. Accordingly, this response is submitted as a complete response to all of the issues raised in the Office Action dated November 22, 2000. In view of remarks traversing rejections, it is asserted that pending claims 17-29 are in condition for allowance. If

the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

The Commissioner is authorized to charge any additional fees that may be required, or credit any overpayment, to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5500-36100.

Respectfully submitted,



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